WHAT IS CLAIMED IS:

1. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by an insulator, the gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator.

2. The transistor of claim 1, wherein the value of x is approximately between 0.5 and 1.0.

3. The transistor of claim 1, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

4. The transistor of claim 1, wherein the insulator is formed of silicon dioxide.

5. The transistor of claim 1, wherein the gate is an electrically isolated floating gate and further comprising a control gate, separated from the floating gate by an intergate dielectric.

6. The transistor of claim 5, wherein the intergate dielectric is formed of silicon dioxide.

7. The transistor of claim 5, wherein the predetermined value x is selected to provide a desired charge retention time of the floating gate.

8. The transistor of claim 5, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the

floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

9. The transistor of claim **8**, wherein the emission of electrons from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

10. The transistor of claim **1**, wherein the gate is formed of a material selected from the group consisting of monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

11. A device for detecting light, the device comprising:

a source region;

a drain region;

a channel region between the source and drain regions; and

a floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the floating gate and the insulator for charge storage upon the floating gate and emission of charge from the floating gate in response to absorbed incident photons.

12. The device of claim **11**, further comprising a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

13. The device of claim **11**, wherein x is selected at a predetermined value that is approximately between 0.5 and 1.0.

14. The device of claim **11**, wherein x is selected at a predetermined value to provide a desired value of the barrier energy that is approximately between 0 eV and 2.8 eV.

15. The device of claim **11**, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

16. The device of claim **11**, wherein the emission of charge from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

17. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator; and

a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

18. The device of claim **17**, wherein the value of x is selected approximately between 0.5 and 1.0.

19. The device of claim **17**, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

20. The device of claim **17**, wherein the value of x is selected to provide a desired charge retention time of the floating gate.

21. A method of producing a transistor on a semiconductor substrate, the method comprising:

forming a source and drain regions, thereby defining a channel region between the source and drain regions;

forming an insulating layer on the channel region; and

forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$; and

selecting x at a predetermined value approximately between 0 and 1.0.

22. The method of claim **21**, wherein x is selected to establish a desired value of a barrier energy between the gate and the insulator.

23. The method of claim **22**, wherein the selected value of x establishes the desired value of the barrier energy approximately between 0 eV and 2.8 eV.

24. The method of claim **21**, wherein x is selected at a predetermined value that is approximately between 0.5 and 1.0.

25. The method of claim **21**, wherein x is selected at a predetermined value that establishes a desired charge retention time.

26. The method of claim **25**, wherein the desired charge retention time is approximately between 1 second and 10^6 years.

27. The method of claim 21, wherein the gate is a floating gate, and x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

28. The method of claim 27, wherein x is selected to provide sensitivity to light selected from the group consisting of infrared light, visible light, and ultraviolet light.

29. The method of claim 21, wherein fabricating the gate includes the steps of:

depositing the silicon carbide compound using low pressure chemical vapor deposition to form a layer of gate material; and

etching the gate material to a desired pattern using a reactive ion etch process.

30. The method of claim 21, wherein etching the gate material further includes using plasma etching in combination with the reactive ion etching.

31. The method of claim 21, further comprising conductively doping the gate material prior to depositing the gate material on the insulating layer.

32. The method of claim 21, further comprising oxidizing the gate material to form a thin layer of oxide on the gate material.

33. The method of claim 21, wherein the gate is a floating gate, and further comprising:

forming a second insulating layer over the floating gate; and

forming a control gate over the second insulating layer.

34. An method of detecting light, the method comprising:

storing charge on a floating gate of a transistor;

receiving incident light at the floating gate, thereby removing at least a portion of the stored charge from the floating gate by the photoelectric effect; and

detecting a change in conductance between the transistor source and drain.

35. The method of claim **34**, further comprising selecting at least one wavelength of the incident light to which the floating gate transistor is most sensitive.

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